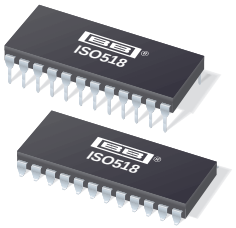
BURR-BROWN®



ISO518

For most current data sheet and other product information, visit www.burr-brown.com

Bidirectional ISOLATED DIGITAL COUPLERS

FEATURES

- LOW POWER CONSUMPTION: < 12mW per Channel
- 1500Vrms ISOLATION: 100% Tested by Partial Discharge
- DOUBLE BUFFERED DESIGN FOR EASY INTEGRATION INTO BUS-BASED SYSTEMS
- TRI-STATE OUTPUTS
- 24-PIN PDIP OR GULL WING PACKAGES
- 2MWORDS/S TRANSFER RATE

APPLICATIONS

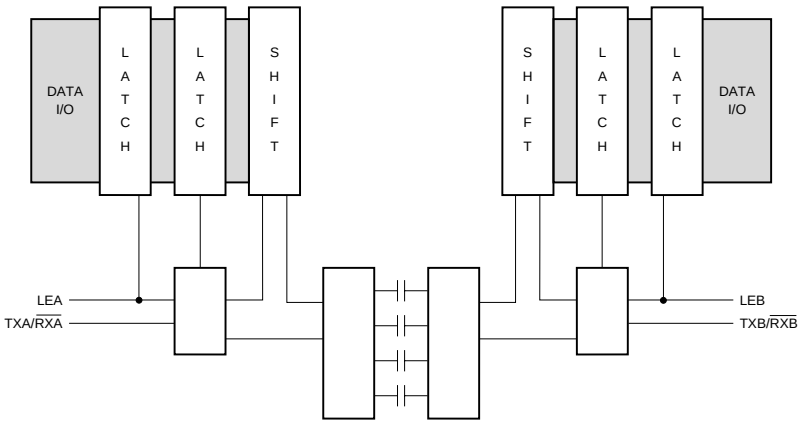
- PARALLEL ADCs/DACs
- DIGITAL INTERFACES
- DIGITAL TRANSMISSION
- GROUND-LOOP ISOLATION

DESCRIPTION

The ISO518 is an 8-channel, isolated, bidirectional digital coupler based on the Burr-Brown capacitive barrier technology.

The ISO518 is designed with input and output buffers for ease of integration into a µP bus system. All data pins are I/O under the control of the TX pins. Input and output buffers are controlled by the latch enable pins. This feature of the ISO518, which allows multiple access to a data bus, requires extra circuitry when using an alternative solution.

The ISO518 will transfer an 8-bit word at rates up to 2Mwords/s without the skew problems associated in implementing this function with optocouplers. The ISO518 is available in 24-pin PDIP or 24-pin Gull Wing packages. Both are specified for operation from –40°C to +85°C.



ISO518 Functional Block Diagram

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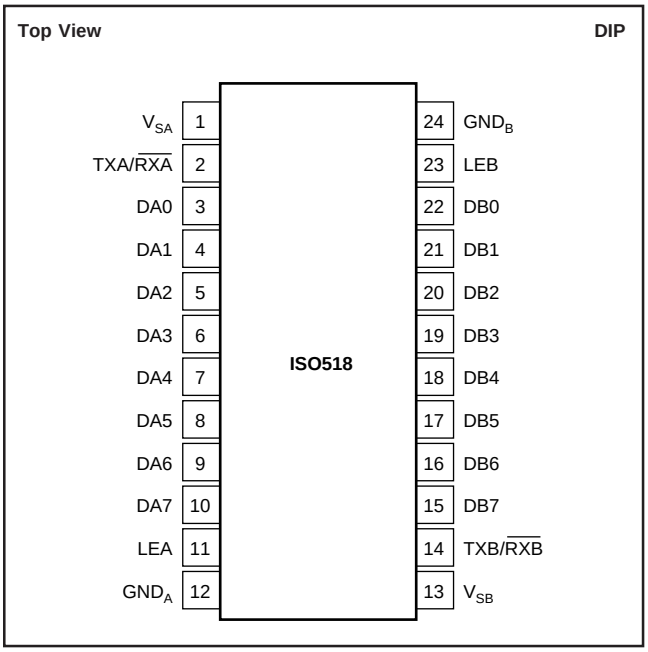
SPECIFICATIONS

At T_A = +25°C, and V_S = +5V, unless otherwise noted.

PARAMETER		CONDITIONS	ISO518P, P-U MIN	ISO518P, P-U TYP	ISO518P, P-U MAX	UNITS
ISOLATION						
Rated Voltage, Continuous	V_{ISO}	50Hz, 60Hz	1500			Vrms
Partial Discharge Voltage		1s, 5 x 5pC/cycle(1)	2500			Vrms
Barrier Impedance				$>10^{14}$ || 10		Ω/pF
Leakage Current		240V, 60Hz		1		µA
		2500V, 50Hz			12	µA
Creepage Distance		PDIP = "P" and "U" Package		11		mm
Internal Isolation Distance		PDIP = "P" and "U" Package		0.1		mm
Transient Recovery Time		5kV/µs Edge			1	µs
DC CHARACTERISTICS						
High Level Input Voltage	V_{IH}	See Note 2	2			V
Low Level Input Voltage	V_{IL}	See Note 2			0.8	V
Input Leakage Current	I_L			5		nA
Input Capacitance	C_{IN}			5		pF
High Level Output Voltage	V_{OH}	I_{OH} = 6mA	V_S –1			V
Low Level Output Voltage	V_{OL}	I_{OL} = 6mA			0.4	V
Output Short-Circuit Current	I_{OS}	I_S, max		30		mA
TIMING						
LE Width (LOW)	t_{WL}		100			ns
LE Width (HIGH)	t_{WH}		15			ns
Data Set-Up to LEA/B	t_{SU}	LEA/B HIGH to LOW	0			ns
Data Hold from LEA/B	t_H	LEA/B HIGH to LOW	20			ns
Propagation Delay	t_{PD}	LEA/B LOW to Data Out			520	ns
Data Output Delay	t_{OD}	LEO HIGH to Data Out Channels			35	ns
Output Rise and Fall Time	t_{RF}	10% to 90% Load = 50pF		9	14	ns
Output Enable	t_{EN}	$\overline{OE}$ to Data Valid HIGH or LOW			35	ns
Output Disable	t_{DIS}	$\overline{OE}$ to Data HI-Z			35	ns
Max Data Transfer Rate			2			Mw/s
Skew		Between Any Two Channels		5		ns
POWER						
Supply Voltage	V_{SA}, V_{SB}	Either Side	4.5		5.5	V
Supply Current	$I_{SA/B}$	Transmit Side DC		5	10	mA
		Transmit Side DC Max Rate		7	15	mA
Supply Current	$I_{SB/A}$	Receive Side DC		8	12	mA
		Receive Side Max Rate		12	20	mA
TEMPERATURE RANGE						
Operating			–40		+85	°C
Storage			–40		+125	°C
Thermal Resistance, θ_{JA}				+75		°C/W

NOTES: (1) All devices receive a 1s test. Failure criterion is > 5pC pulses of ≥ 5pC per cycle. (2) Logic inputs are HCT-type and thresholds are a function of power supply voltage with approximately 400mV hysteresis.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage: V_{SA}	–0.5V to +6V
V_{SB}	–0.5V to +6V
Maximum Input Current, Any Input	20mA
Continuous Isolation Voltage	1500Vrms
Storage Temperature	–40°C to +125°C
Lead Temperature (soldering, 10s)	300°C

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
ISO518P	24-Pin Plastic DIP	167
ISO518P-U	24-Pin Gull Wing Surface Mount	167-4

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

FUNCTIONAL DESCRIPTION

NAME	FUNCTION
DA (0 - 7)	Data Bus A. The logic levels on these pins are transmitted to, or received from the corresponding pins on data bus B.
DB (0 -7)	Data Bus B. The logic levels on these pins are transmitted to, or received from the corresponding pins on data bus A.
LEA(1)	Latch Enable A. Latch enable signal for the A data buffer.
LEB(1)	Latch Enable B. Latch enable signal for the B data buffer.
TX/$\overline{RX}$A(2)	Transmit/Receive Control for Side A.
TX/$\overline{RX}$B(2)	Transmit/Receive Control for Side B.

NOTES: (1) In transmit mode (TX/$\overline{RX}$ = 1), a logic 0 (LOW) will latch the input buffer data into the input register and initialize the transmission. A logic 0 (LOW) will latch the internal buffer data into the output register and prevent any further changes in the output data. A logic 1 (HIGH) will pass the internal buffer data to the output register and permit each new set of data to appear as soon as available after transmission. (2) A logic 1 (HIGH) will set that side to transmit mode and the same side's data bus to input mode. A logic 0 (LOW) will set that side to receive mode and the same side's data bus to output mode.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

OPERATION

Data is transmitted across the barrier under the control of LEA or LEB; the direction being decided by TXA/$\overline{\text{RXA}}$ and TXB/$\overline{\text{RXB}}$.

Assume side A is set to transmit and side B is set to receive. With LEA LOW, no data is passed to the input buffer and no barrier transmission takes place. When LEA is HIGH, the input data is passed to the input buffer ready for transmission across the barrier on the falling edge of LEA. On the falling edge of LEA, the data is latched to prevent any subsequent input data changes interfering with the single barrier transmission. Should LEA go HIGH again before the transmission is complete, the data in the input pins will be loaded into the input buffer without affecting the transmission. However, should LEA go LOW again before the barrier transmission is complete, the barrier transmission will terminate and restart with the new data (see Figure 2). This will not affect the output data which only changes at the end of a transmission or under control of LEB.

If LEB is HIGH, the output data will change at the end of transmission. If LEB is LOW the output data will change when LEB next goes HIGH. In both cases, all data bits will change together, guaranteeing the specified skew performance. It should also be noted that LEB may be used to ignore transmitted data if required.

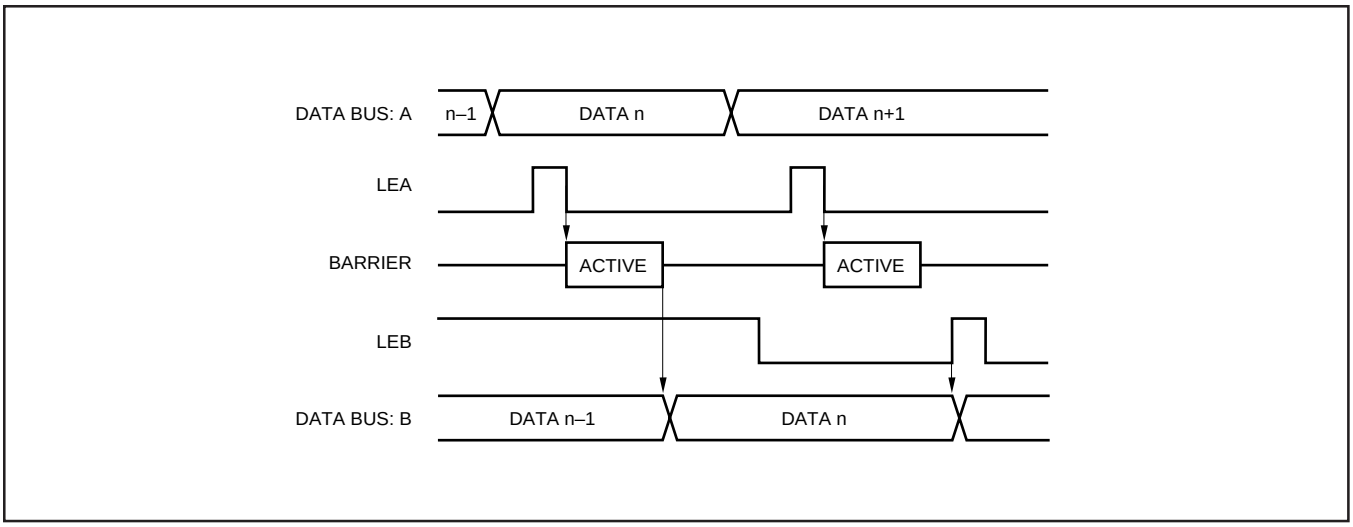


FIGURE 1. Data Transfer.

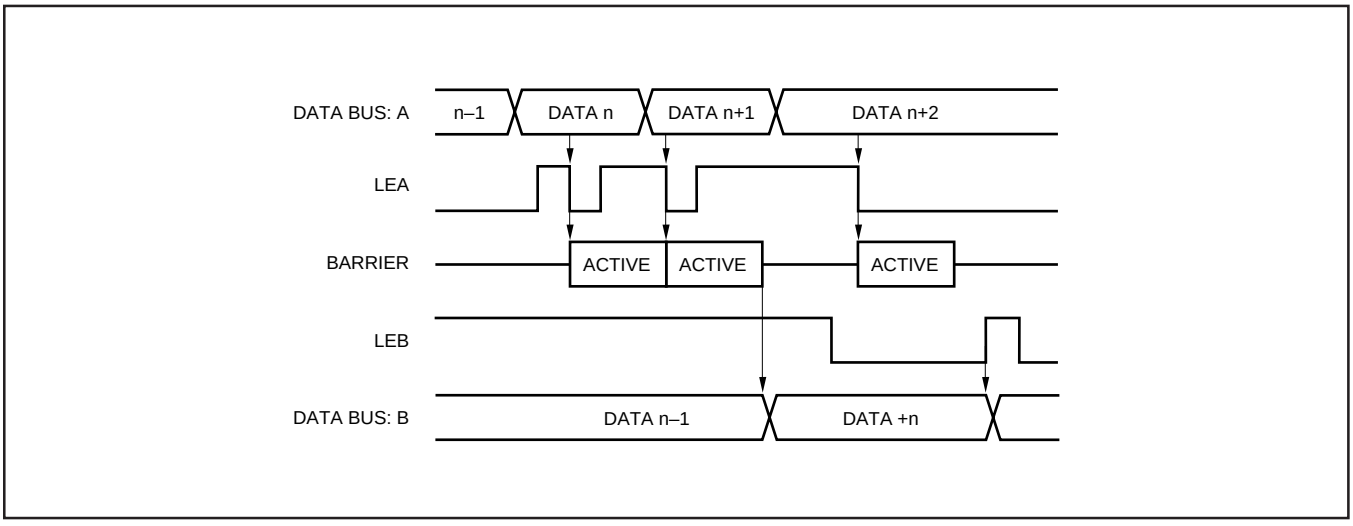


FIGURE 2. Data Transfer—Restart.

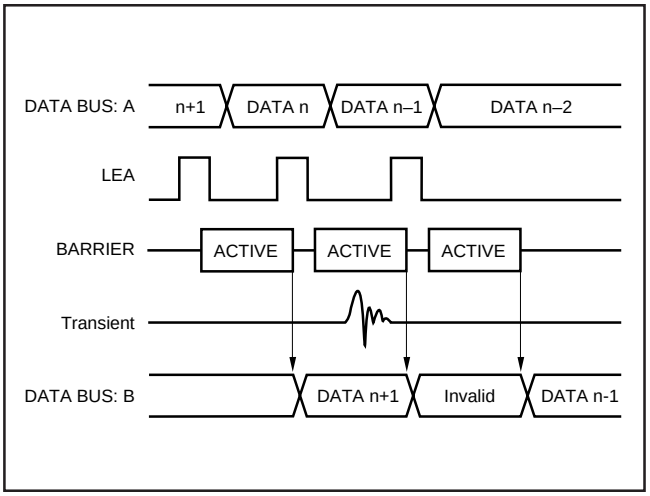


FIGURE 3. Data Corruption.

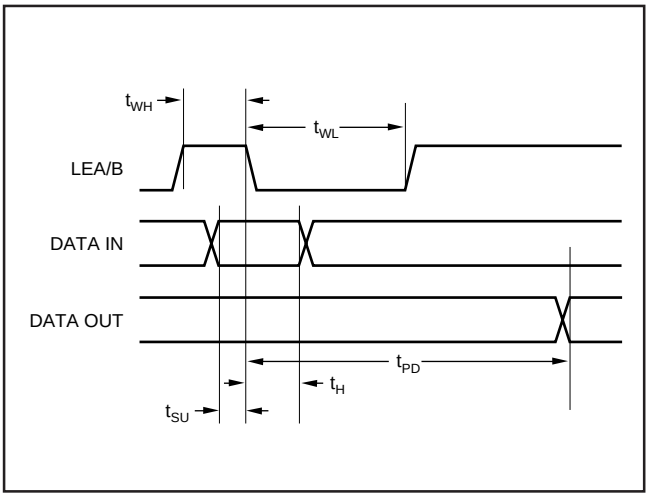


FIGURE 4. Transmission Timing Diagram.

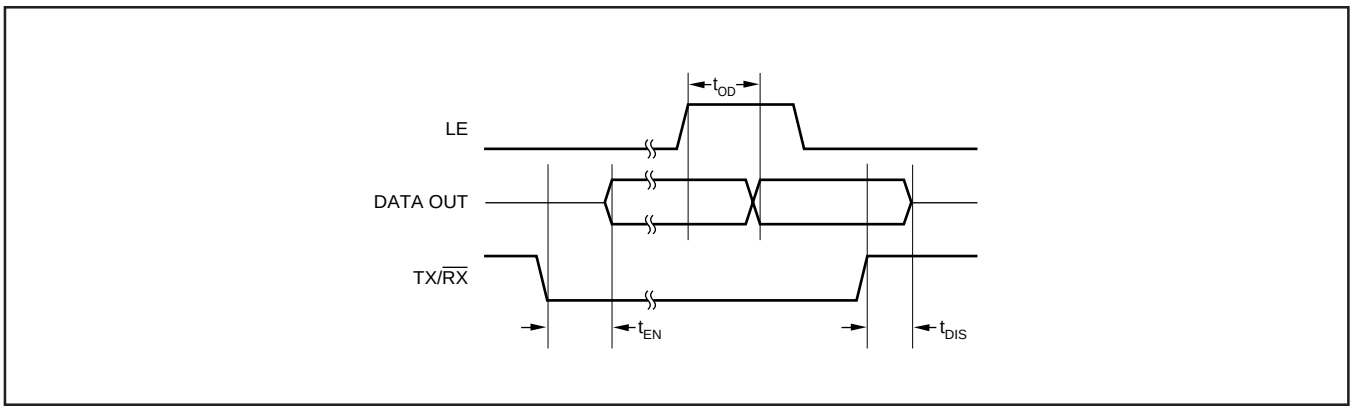


FIGURE 5. Output Data Timing.

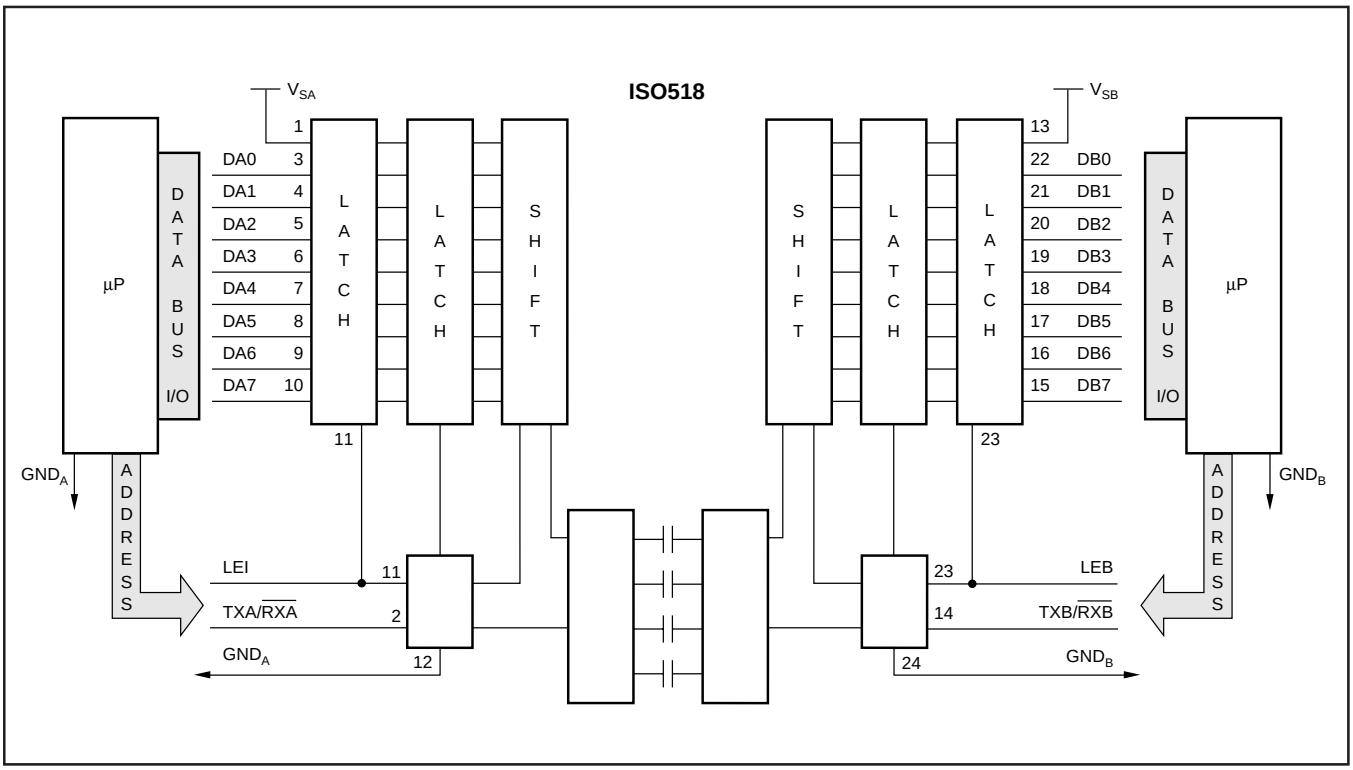


FIGURE 6. Burr-Brown I/O System using ISO518.

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